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(54) **ARRAY SUBSTRATE, ELECTROLUMINESCENT DISPLAY PANEL AND DISPLAY DEVICE**

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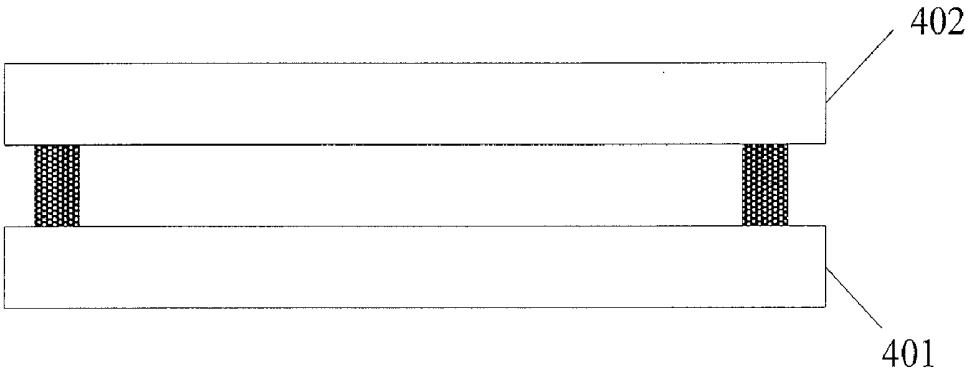
(57) **ABSTRACT**

An array substrate, an electroluminescent display panel, and a display device are disclosed. The array substrate includes: a base substrate, and a first signal line, an insulating layer and a second signal line provided sequentially on the base substrate in a direction perpendicular to the base substrate; wherein the first signal line has a first portion and a second portion, the first portion has a resistance higher than a resistance of the second portion, and at least a part of the first portion is overlapped with the second signal line, and the second portion is non-overlapped with the second signal line.



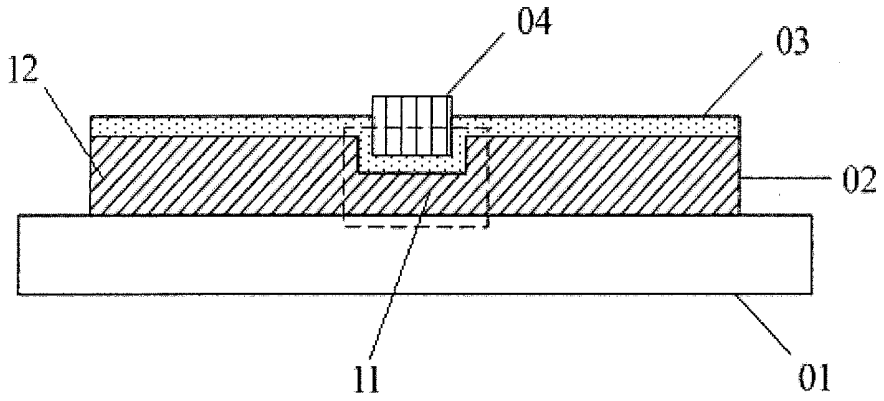


FIG. 1A

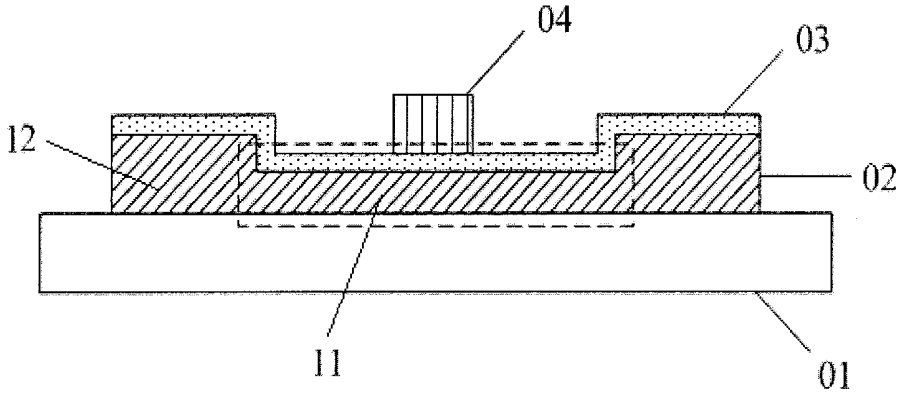


FIG. 1B

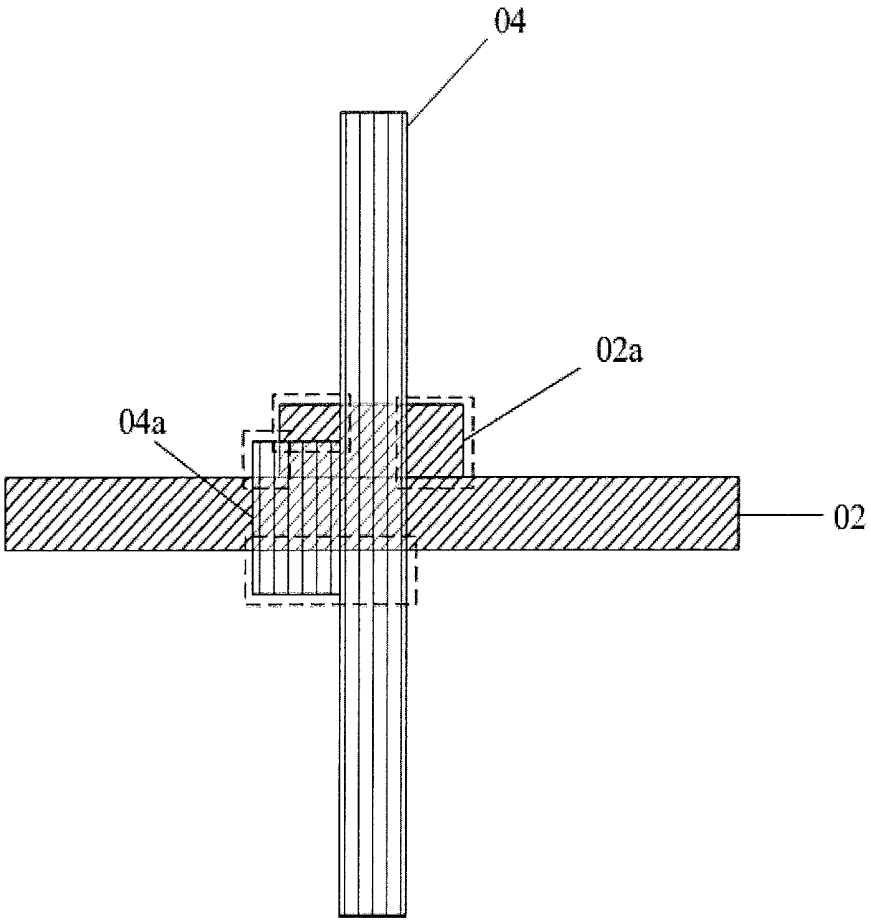


FIG. 2A

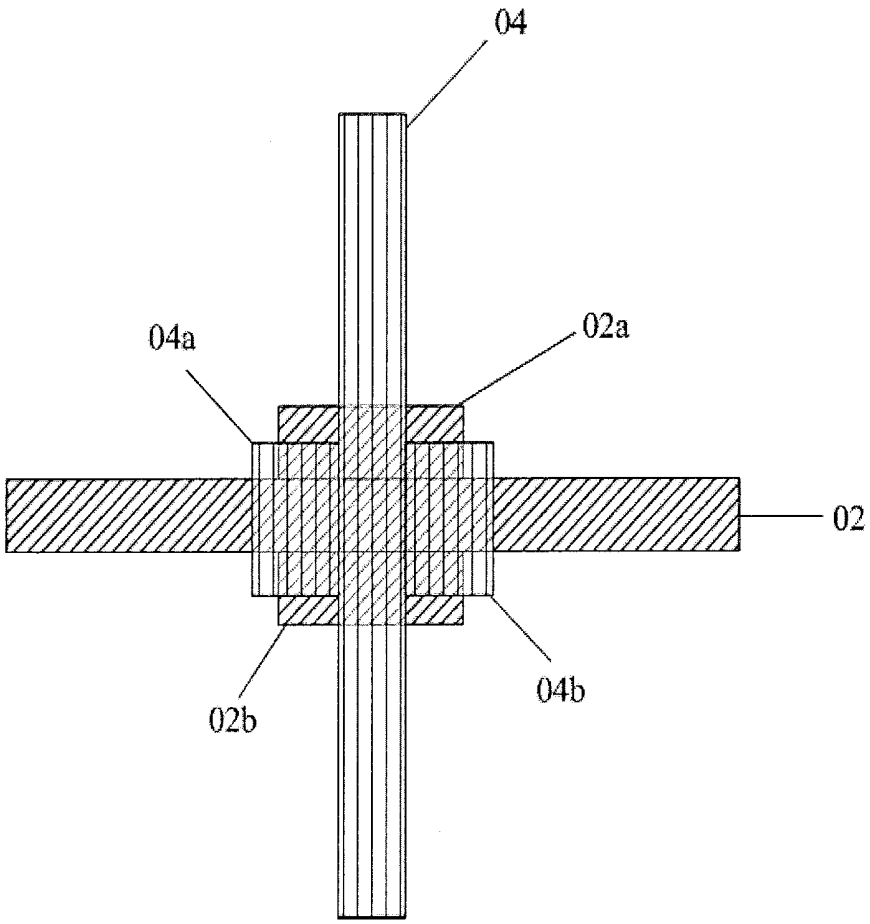


FIG. 2B

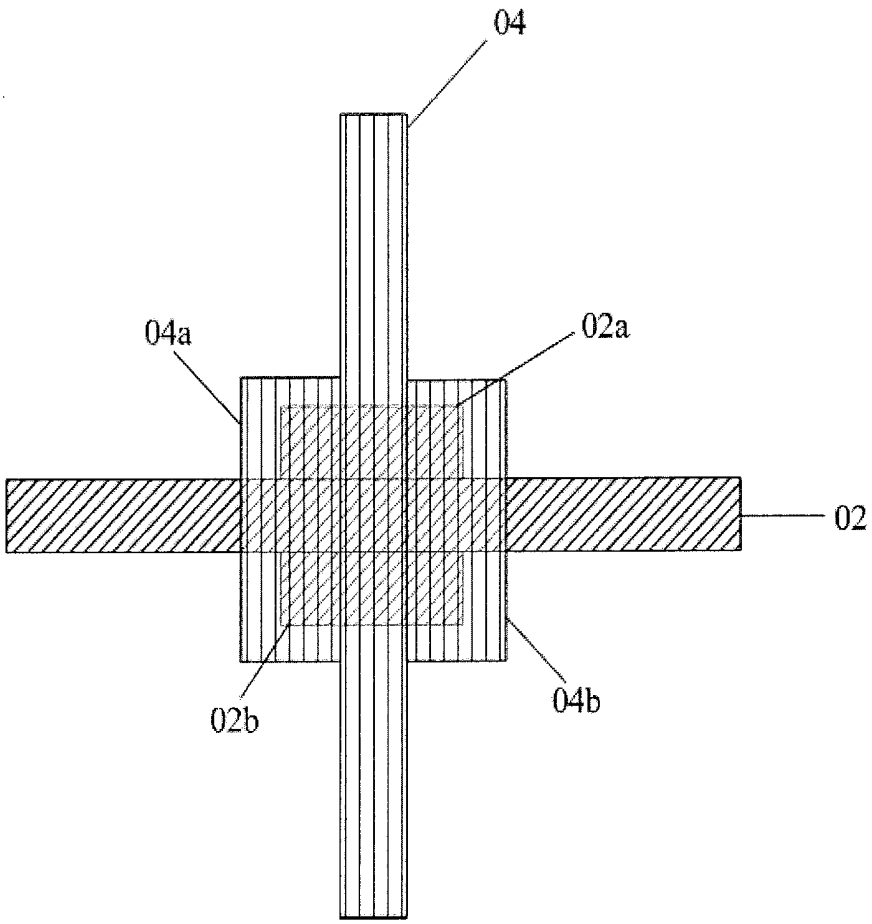


FIG. 2C

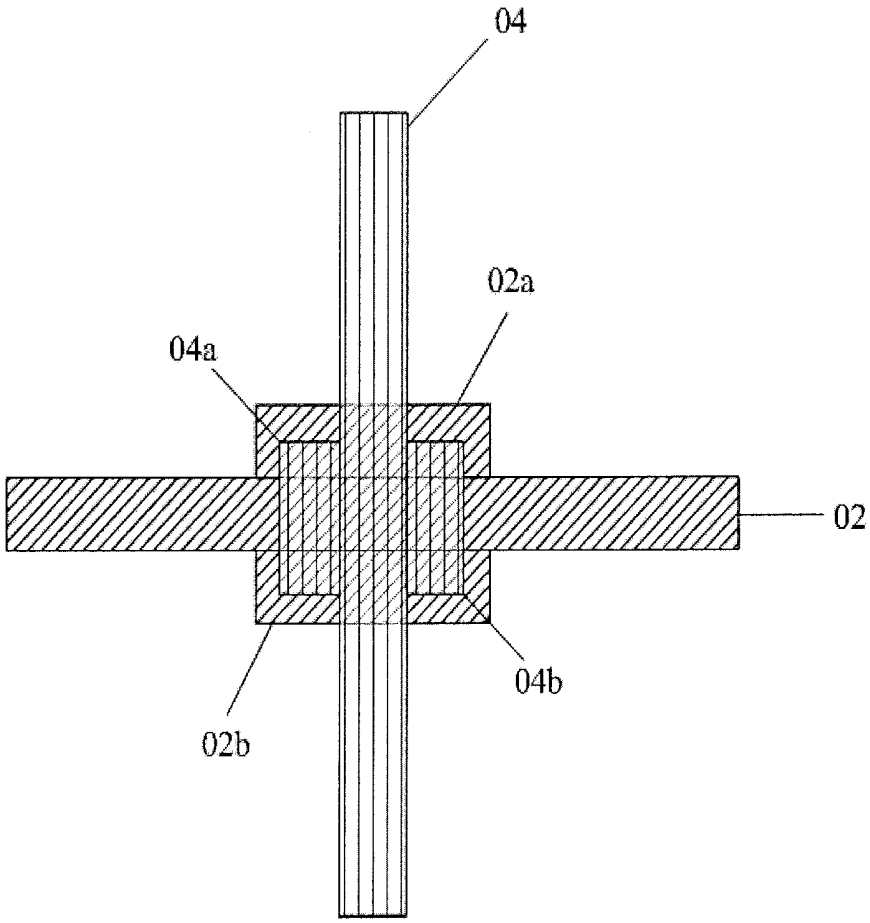


FIG. 2D

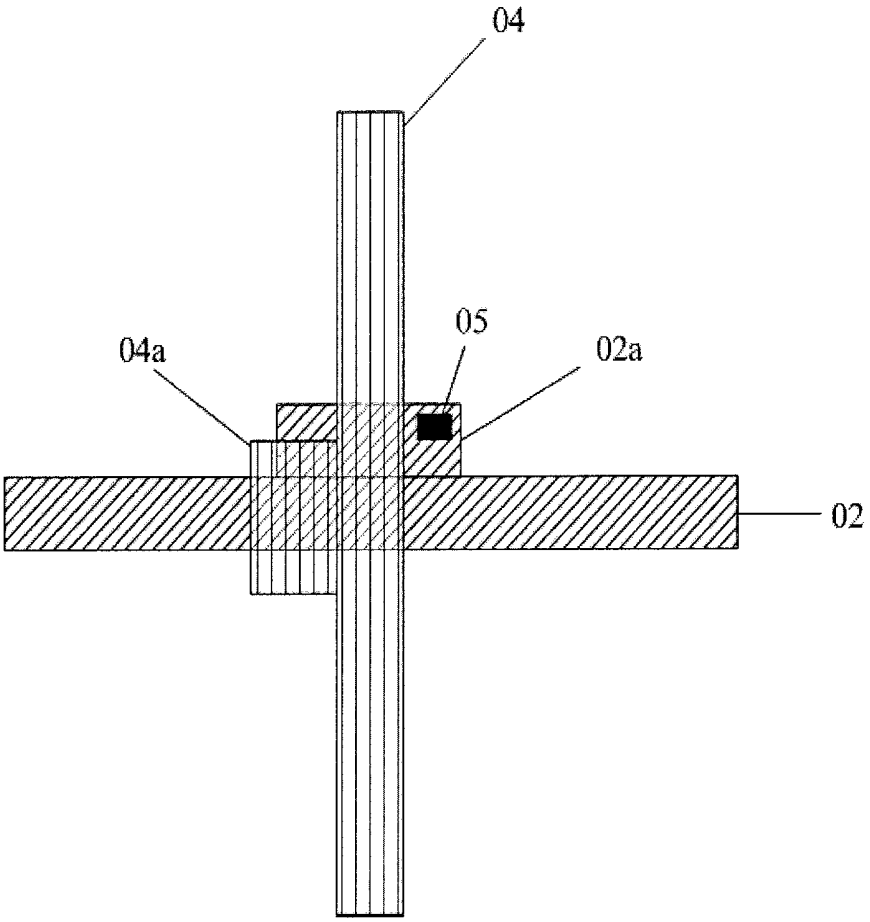


FIG. 3A

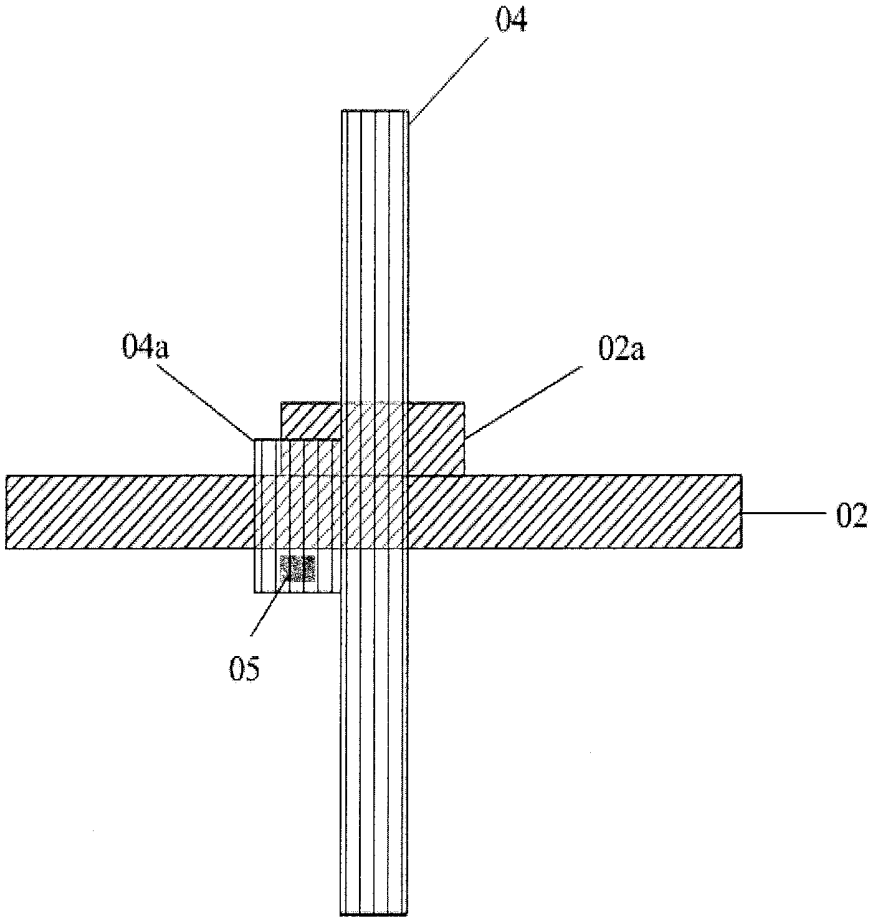


FIG. 3B

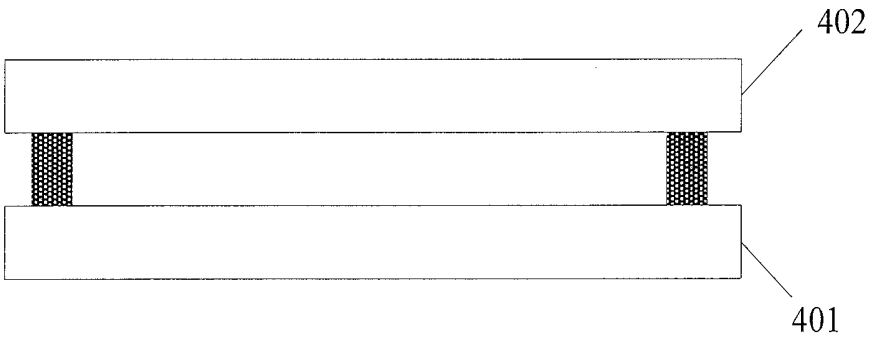


FIG. 4

ARRAY SUBSTRATE, ELECTROLUMINESCENT DISPLAY PANEL AND DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a Section 371 National Stage Application of International Application No. PCT/CN2018/079992, filed on Mar. 22, 2018, entitled "Array Substrate, Electroluminescent Display Panel and Display Device", which published as WO 2018/219025 A1on 6 Dec. 2018, which claims priority to Chinese Application No. 201720633454.1, filed on 2 Jun. 2017 with CNIPA, incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to display technical field, more particularly, to an array substrate, an electroluminescent display panel and a display device.

BACKGROUND

[0003] An Organic Light Emitting Diode (OLED) display panels, according to driving modes, may be divided into Passive Matrix OLED (PMOLED) display panel and Active Matrix OLED (AMOLED) display panel. The AMOLED display panel has pixels arranged in an array, belongs to an active display type, has advantages of high emission efficiency, high contrast, wide visual angle, and the like, and is generally applied to a high-resolution display device with large scale.

SUMMARY

[0004] An embodiment of the present disclosure provides an array substrate, including: a base substrate; and a first signal line, an insulating layer and a second signal line provided sequentially on the base substrate in a direction perpendicular to the base substrate, wherein the first signal line has a first portion and a second portion, the first portion having a resistance higher than a resistance of the second portion, at least a part of the first portion being overlapped with the second signal line, and the second portion non-overlapped with the second signal line.

[0005] In some embodiments, the first portion of the first signal line includes a portion of the first signal line completely overlapped with the second signal line.

[0006] In some embodiments, the first portion of the first signal line is completely overlapped with the second signal line.

[0007] In some embodiments, the first portion of the first signal line has a smaller thickness than the second portion of the first signal line.

[0008] In some embodiments, the insulating layer has a same thickness at a location on the first portion of the first signal line as that at a location on the second portion of the first signal line.

[0009] In some embodiments, the first portion of the first signal line includes a first extension overlapped with the second signal line and extending in a widthwise direction of the first portion, and the second signal line includes a second extension overlapped with the first signal line and extending in a widthwise direction of the second signal line; wherein an orthographic projection of the first extension onto the base substrate has an area overlapped with an orthographic projection of the second extension onto the base substrate.

[0010] In some embodiments, the first extension has a same thickness as the portion of the first signal line completely overlapped with the second signal line.

[0011] In some embodiments, the orthographic projections of the first extension and the second extension onto the base substrate are partly overlapped with each other.

[0012] In some embodiments, the array substrate further includes a metal electrode connected with the first extension or the second extension, wherein an orthographic projection of the metal electrode onto the base substrate is at most overlapped with the orthographic projection of one of the first extension and the second extension onto the based substrate.

[0013] In some embodiments, the metal electrode is located between a layer where the first signal line is located and the insulating layer; and the meal electrode is electrically connected with the first extension.

[0014] In some embodiments, the metal electrode is located between the insulating layer and a layer where the second signal line is located; and the meal electrode is electrically connected with the second extension.

[0015] In some embodiments, the first signal line is a low-level voltage signal line, and the second signal line is a high-level voltage signal line.

[0016] An embodiment of the present disclosure further provides an electroluminescent display panel, including the array substrate as described in any one of the above embodiments.

[0017] An embodiment of the present disclosure further provides a display device, including the electroluminescent display panel as described in any one of the above embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIGS. **1**A and **1**B are side views of an array substrate provided in an embodiment of the present disclosure, respectively;

[0019] FIGS. **2**A to **2**D are top views of a first signal line and a second signal line provided in an embodiment of the present disclosure, respectively;

[0020] FIGS. **3**A and **3**B are schematic views showing positions of metal electrodes provided in an embodiment of the present disclosure, respectively; and

[0021] FIG. **4** is a schematic view showing a structure of an electroluminescent display panel provided in an embodiment of the present disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

[0022] Detailed descriptions of an array substrate, an electroluminescent display panel and a display device provided by embodiments of the present disclosure will be described in detail with reference to the drawings. It is apparent that the described embodiments are only a part of the embodiments of the present disclosure, rather than all the embodiment of the present disclosure. On the basis of the embodiments of the present disclosure, all of other embodiments that can be obtained by the skilled person in the art without any creative efforts also belong to the scope of the present disclosure.

[0023] The inventors have recognized: with the development of the integrated and ultrathin display devices, a

thickness of each film layer on the array substrate in the AMOLED display, especially a thickness of an insulating film layer, tends to a limit, which inevitably causes a decrease in quality of the resulting insulating film layer. When signal lines on upper and lower surfaces of the insulating film layer are respectively inputted into a signal with a large voltage difference, especially the largest voltage difference between a high-level voltage signal VDD and a low-level voltage signal VSS, the signals are easy to break down the insulating layer in an area intersecting with the signal lines, causing an occurrence of a short circuit between the upper and lower signal lines so as to affect the display effect.

[0024] An embodiment of the present disclosure provides an array substrate, as shown in the side views of FIGS. **1**A and **1**B, including: a base substrate **01** (a white-filled area), and a first signal line **02** (a slash-filled area), an insulating layer **03** (a black dot-filled area) and a second signal line **04** (a vertical line-filled area) provided sequentially on the base substrate **01** in a direction perpendicular to the base substrate **01**; and the first signal line **02** intersects with the second signal line **04**. The first signal line **02** has a first portion **11** and a second portion **12**. A resistance of the first portion **11** is higher than that of the second portion **12**. At least a part of the first portion **11** overlaps with the second signal line **04**, but the second portion **12** does not overlap with the second signal line **04**. In other words, a portion of the first signal line **02** completely overlapped with the second signal line **04** is provided in the first portion **11**. The first portion **11** may only include the portion of the first signal line **02** completely overlapped with the second signal line **04** in the direction perpendicular to the base substrate. Alternatively, the first portion **11** may also include other portions, for example, portions adjacent to the portion of the first signal line **02** completely overlapped with the second signal line **04**. Herein, for example, an orthographic projection of the portion of the first signal line **02** completely overlapped with the second signal line **04** onto the base substrate **01** completely falls within an orthographic projection of the second signal line **04** onto the base substrate **01**.

[0025] As an example, the resistance of the first portion **11** of the first signal line **02** may be greater than that of other portions of the first signal line **02**.

[0026] In the above-mentioned array substrate provided by an embodiment of the present disclosure, in order to prevent short circuit in the overlapping area (or intersecting area) of the first and second signal lines located on the upper and lower surfaces of the insulating layer respectively, the resistance of the first portion **11** of the first signal line including the overlapping area is arranged to be greater than that of a non-overlapping portion (for example, the second portion **12**) of the first signal line. That is, the resistance of the first portion of the first signal line is increased, such that a high resistance region is formed in the portion of the first signal line overlapped with the second signal line, and thus the current in the second signal line is slowed down when it flows through the overlapping area. This avoids a short circuit between the first and second signal lines due to the breakdown of the insulating layer caused by large transient current in the overlapping area flowing through the insulating layer, so as to effectively reduce the probability of the first signal line and the second signal line being short-circuited in the intersecting area, thereby improving the quality of the display picture.

[0027] Specifically, in order to effectively avoid the occurrence of a short circuit between the first signal line and the second signal line, generally, a range of the high resistance region is set to be larger than the area where the first signal line and the second signal line are completely overlapped with each other, as shown in a dashed box of FIG. **1**B. Of course, as shown in a dashed box of FIG. **1**A, it may also be that the range of the high resistance region is equal to the range in which the first and second signal lines are completely overlapped with each other, which is not limited herein.

[0028] It should be noted that, generally in an electroluminescent display panel, a signal line for transmitting signals on an array substrate is usually made of a transparent conductive oxide such as indium tin oxide (ITO). However, it is well known that in the event that ITO is used to form the signal line for transmitting a signal, its own resistance is much higher than resistance of metal. Therefore, normally, in order to improve the conductive property of the ITO signal line, the signal line may customarily be made thicker, that is, the greater the thickness is, the less the resistance becomes, and the better the conductive property becomes; alternatively, the thinner the thickness is, the greater the resistance becomes and the poorer conductive property becomes.

[0029] In a specific implementation, in the electroluminescent display panel, especially in the OLED display panel, a plurality of signal lines for transmitting a low-level voltage (such as VSS) and a plurality of signal lines for transmitting a high-level voltage (such as VDD)are typically arranged on the array substrate. The plurality of signal lines for transmitting the low-level voltage and a plurality of signal lines for transmitting the high-level voltage provide holes and electrons for a light emitting layer for emitting light in the array substrate, respectively. The holes and electrons are recombined in the light emitting layer to emit light, thereby achieving the display. Therefore, in the above array substrate provided by an embodiment of the present disclosure, the first signal line **02** may be a low-level voltage signal line, that is, VSS, and the second signal line **04** may be a high-level voltage signal line, that is, VDD.

[0030] Specifically, in the OLED display panel, when the first signal line **02** is the low-level voltage signal line and the second signal line **04** is the high-level voltage signal line, the first signal line **02** and the second signal line **04** are generally formed of a transparent conductive oxide (such as ITO). Therefore, in order to realize that the resistance of the portion of the first signal line **02** overlapped with the second signal line is greater than the resistance of the non-overlapping portion, in the above-mentioned array substrate provided by an embodiment of the present disclosure, the thickness of the first portion **11** of the first signal line is smaller than that of the second portion **12** of the first signal line. By thinning the thickness of the first portion **11** of the first signal line **02**, the resistance of the overlapping portion of the first signal line **02** is increased, and thus a high resistance region is formed, as shown in FIGS. **1**A and **1**B.

[0031] Specifically, since the insulating layer is only used to insulate the first signal line **02** from the second signal line **04**, the thickness of the insulating layer is generally uniformly disposed, that is, the thickness is kept uniform. Therefore, in the above-mentioned array substrate provided by an embodiment of the present disclosure, the insulating layer has the same thickness at a location on the first portion

of the first signal line as the thickness of the insulating layer at a location on the second portion of the first signal line. As an example, as shown in FIGS. **1**A and **1**B, the thickness of the insulating layer **03** is kept uniform.

[0032] In a specific implementation, in order to slow down the flow velocity of the current in the second signal line flowing through the overlapping area, a buffer capacitor may be formed in the overlapping area to slow down the flow of the current. Specifically, in the above-mentioned array substrate provided by an embodiment of the present disclosure, the part of the first portion of the first signal line overlapped with the second signal line has a first extension, and part of the second signal line overlapped with the first signal line has a second extension. The first extension extends in a widthwise direction of the first portion, and the second extension extends in a widthwise direction of the second signal line.

[0033] An orthographic projection of the first extension onto the base substrate has an overlapping area overlapped with an orthographic projection of the second extension onto the base substrate.

[0034] As an example, the first extension has the same thickness as the portion of the first signal line completely overlapped with the second signal line.

[0035] As an example, as shown in FIG. **2**A to FIG. **2**D, for the convenience of display, the position of the insulating layer is not shown in the figures. The first portion **11** of the first signal line **02** may have one first extension (a first extension **02***a* as shown in FIG. **2**A), and may also have two first extensions (a first extension **02***a* and a first extension **02***b* as shown in FIGS. **2**B to **2**D). A shape of the first extension portion (including the first extension **02***a* and the first extension **02***b*) may be square (as shown in FIGS. **2**A to **2**D), and may also be semi-circular or triangular. Of course, other shapes may be used, which are not limited herein.

[0036] Specifically, as shown in FIG. **2**A to FIG. **2**D, the part of the second signal line **04** overlapped with the first signal line may also have one second extension (a second extension **04***a* as shown in FIG. **2**A), and may also have two second extensions (a second extension **04***a* and a second extension **04***b* as shown in FIGS. **2**B to **2**D). And, for example, the second extension (including the second extension **04***a* and the second extension **04***b*) may have the same shape as the first extension (as shown in FIGS. **2**A to **2**D), alternatively may have a shape different from that of the first extension as long as it is ensured that orthographic projections of the first and second extensions onto the base substrate have an overlapping area to form a buffer capacitor, which is not limited herein.

[0037] As an example, a relationship between the first extension and the second extension may be as shown in FIGS. **2**A to **2**D. The orthographic projection of the first extension (including the first extension **02***a* and the first extension **02***b*) onto the base substrate may have a partly overlapping area with the orthographic projection of the second extension (including the second extension **04***a* and the second extension **04***b*) onto the base substrate, as shown in FIGS. **2**A and **2**B. Of course, the orthographic projection of the first extension (including the first extension **02***a* and the first extension **02***b*) onto the base substrate may also be completely enclosed by the orthographic projection of the second extension (including the second extension **04***a* and the second extension **04***b*) onto the base substrate, as shown in FIG. **2**C. Of course, the orthographic projection of the first extension (including the first extension **02***a* and the first extension **02***b*) onto the base substrate may also completely enclose the orthographic projection of the second extension (including the second extension **04***a* and the second extension **04***b*) onto the base substrate, as shown in FIG. **2**D. Specifically, it may be designed accordingly as required, which is not specifically limited herein.

[0038] Further, since the first signal line and the second signal line respectively have extensions, a buffer capacitor may be formed between the first extension and the second extension, so that the flow velocity of the current in the second signal line may be slowed down when the current flows through the intersecting area, reducing the probability that the first signal line and the second signal line are short-circuited in the intersecting area. However, the formation of the buffer capacitor in fact increases the area of the area of the first signal line overlapped with the second signal line, thereby increasing an area where the current flows, which actually has a certain conflict with the role of the high resistance region. In order to avoid such conflict and to fully utilize the roles of the high resistance region and the buffer capacitor, it is required to simulate the extent where the first signal line is thinned in the intersecting area and the area of the buffer capacitor to obtain an optimal solution to finally reduce the probability of the first signal line and the second signal line being short-circuited in the intersecting area. Consequently, the extent where the first signal line is thinned in the intersecting area and the area of the buffer capacitor are not specifically limited herein.

[0039] In the specific implementation, when the first signal line and the second signal line are made of a transparent conductive oxide (such as ITO), since the resistance of the transparent conductive oxide is great, it is easy to cause great voltage difference when the current flows through the signal lines, to affect the light-emitting effect, and thus affecting the display effect. In order to avoid this situation, for example, a metal electrode may be fabricated on the surface of the first signal line or the second signal line as an auxiliary electrode to reduce the voltage difference. Meanwhile, in order not to affect the roles of the high resistance region and the buffer capacitor that the velocity of the current in the second signal line is slowed down in the overlapping area and the probability of the first signal line and the second signal line being short-circuited in the overlapping area is lowered, in the above-mentioned array substrate provided by an embodiment of the present disclosure, as an example, when the orthographic projections of the first extension and the second extension onto the base substrate are only partially overlapped with each other, the array substrate may further include: a metal electrode disposed on and outside the overlapping area (i.e., an orthographic projection of the metal electrode onto the base substrate is at most overlapped with the orthographic projection of one of the first signal line **02** and the second signal line **04** onto the base substrate, or the orthographic projection of the metal electrode onto the base substrate may be overlapped with the orthographic projection of the first signal line **02** onto the base substrate, or may be overlapped with the orthographic projection of the second signal line **04** onto the base substrate, or may be overlapped with none of the orthographic projections of the first signal line **02** and the second signal line **04** onto the base substrate), and the metal electrodes are connected with the first extension or the second extension. As shown in FIG.

2A, the metal electrode may be generally located in the non-intersecting area, the non-overlapping area, and a non-overlapping area of the second extension **04***a* with the first signal line **02**. That is, the metal electrode may be located within the dashed box, such that in the case of ensuring the roles of the high resistance region and the buffer capacitor, the role of the metal electrode may be realized in order to prevent mutual interference therebetween.

[0040] Specifically, in the above-mentioned array substrate provided by an embodiment of the present disclosure, the metal electrode may be disposed between a layer where the first signal line is located and a layer where the second signal line is located (for example, a film layer between the layer where the first signal line is located and the layer where the second signal line is located) and may be electrically connected with the first signal line or the second signal line according to a specific position; wherein when the metal electrode **05** is located between the layer where the first signal line **02** is located and the insulating layer **03** (for example, the film layer between the layer where the first signal line **02** is located and the insulating layer **03**), as shown in FIG. **3**A, the metal electrode **05** (a black-filled area) is electrically connected with the first extension **02***a*.

[0041] Alternatively, in the above-mentioned array substrate provided by an embodiment of the present disclosure, when the metal electrode **05** is located between the insulating layer **03** and the layer where the second signal line **04** is located (for example, the film layer between the insulating layer **03** and the layer where the first signal line **04** is located), as shown in FIG. **3**B, the metal electrode **05** (a black-filled area) is electrically connected with the second extension **04***a*.

[0042] Of course, the metal electrode is not limited to be disposed in the film layer between the layer where the first signal line is located and the layer where the second signal line is located, and may be disposed at other positions as required, which is not limited herein.

[0043] On the basis of the same concept, an embodiment of the present disclosure further provides an electroluminescent display panel. As shown in FIG. **4**, it may include: the above array substrate **401** provided in an embodiment of the present disclosure, and may include a package substrate **402** disposed opposite to the array substrate. As an example, the array substrate **401** may be fixed with the package substrate **402** by, for example, glue bonding or mechanical connector.

[0044] On the basis of the same concept, an embodiment of the present disclosure further provides a display device. It may include the above electroluminescent display panel as provided by an embodiment of the present disclosure. The display device may be a mobile phone, a tablet computer, a television, a display, a notebook computer, a digital camera, a navigator, or any product or component having a display function. The specific implementation may make reference to the descriptions for the above-mentioned electroluminescent display panel provided by the embodiment of the present disclosure. The same contents will not be repeated.

[0045] Embodiments of the present disclosure provide an array substrate, an electroluminescent display panel, and a display device. The array substrate includes: a base substrate, and a first signal line, an insulating layer and a second signal line provided sequentially on the base substrate; the first signal line has a first portion and a second portion, the resistance of the first portion is higher than that of the second portion. At least a part of the first portion is overlapped with the second signal line, and the second portion is not overlapped with the second signal line. In order to prevent a short circuit in the overlapping area of the first and second signal lines located on the upper and lower surfaces of the insulating layer, the resistance of the first portion of the first signal line including the overlapping area may be arranged to be greater than that of a non-overlapping portion of the first signal. That is, the resistance of the overlapping area of the first signal line is increased, such that a high resistance region is formed in the overlapping area of the first signal line with the second signal line, and thus the flow velocity of the current in the second signal line is slowed down when the current flows through the overlapping area. This efficiently avoids a short circuit between the first and second signal lines due to the breakdown of the insulating layer caused by large transient current in the overlapping area flowing through the insulating layer, so as to effectively reduce the probability of short-circuit of the first signal line and the second signal line in the intersecting area, thereby improving the quality of the display picture.

[0046] It would be apparent by those skilled in the art that various modifications and variations may be made to these embodiments of the present disclosure without departing from the principle and scope of the present disclosure. In this way, if the modifications and variations made to the present disclosure belong to the scope of which is defined in the claims and their equivalents, the present disclosure is intended to encompass the modifications and variations.

1. An array substrate, comprising:

a base substrate; and

a first signal line, an insulating layer and a second signal line provided sequentially on the base substrate in a direction perpendicular to the base substrate,

wherein the first signal line has a first portion and a second portion, the first portion having a resistance higher than a resistance of the second portion, at least a part of the first portion being overlapped with the second signal line, and the second portion non-overlapped with the second signal line.

2. The array substrate as claimed in claim **1**, wherein the first portion of the first signal line comprises a portion of the first signal line completely overlapped with the second signal line.

3. The array substrate as claimed in claim **1**, wherein the first portion of the first signal line is completely overlapped with the second signal line.

4. The array substrate as claimed in claim **1**, wherein the first portion of the first signal line has a smaller thickness than the second portion of the first signal line.

5. The array substrate as claimed in claim **4**, wherein the insulating layer has a same thickness at a location on the first portion of the first signal line as that at a location on the second portion of the first signal line.

6. The array substrate as claimed in claim **4**, wherein the first portion of the first signal line comprises a first extension overlapped with the second signal line and extending in a widthwise direction of the first portion, and the second signal line comprises a second extension overlapped with the first signal line and extending in a widthwise direction of the second signal line;

wherein an orthographic projection of the first extension onto the base substrate has an area overlapped with an orthographic projection of the second extension onto the base substrate.

7. The array substrate as claimed in claim **6**, wherein the first extension has a same thickness as the portion of the first signal line completely overlapped with the second signal line.

8. The array substrate as claimed in claim **6**, wherein the orthographic projections of the first extension and the second extension onto the base substrate are partly overlapped with each other.

9. The array substrate as claimed in claim **8**, further comprising a metal electrode connected with the first extension or the second extension, wherein an orthographic projection of the metal electrode onto the base substrate is at most overlapped with the orthographic projection of one of the first extension and the second extension onto the based substrate.

10. The array substrate as claimed in claim **9**, wherein the metal electrode is located between a layer where the first signal line is located and the insulating layer; and the meal electrode is electrically connected with the first extension.

11. The array substrate as claimed in claim **9**, wherein the metal electrode is located between the insulating layer and a layer where the second signal line is located; and the meal electrode is electrically connected with the second extension.

12. The array substrate as claimed in claim **1**, wherein the first signal line is a low-level voltage signal line, and the second signal line is a high-level voltage signal line.

13. An electroluminescent display panel comprising the array substrate as claimed in claim **1**.

14. A display device comprising the electroluminescent display panel as claimed in claim **13**.

15. The electroluminescent display panel as claimed in claim **13**, wherein the first portion of the first signal line comprises a portion of the first signal line completely overlapped with the second signal line.

16. The electroluminescent display panel as claimed in claim **13**, wherein the first portion of the first signal line is completely overlapped with the second signal line.

17. The a electroluminescent display panel as claimed in claim **13**, wherein the first portion of the first signal line has a smaller thickness than the second portion of the first signal line.

18. The electroluminescent display panel as claimed in claim **17**, wherein the insulating layer has a same thickness at a location on the first portion of the first signal line as that at a location on the second portion of the first signal line.

19. The electroluminescent display panel as claimed in claim **17**, wherein the first portion of the first signal line comprises a first extension overlapped with the second signal line and extending in a widthwise direction of the first portion, and the second signal line comprises a second extension overlapped with the first signal line and extending in a widthwise direction of the second signal line;

wherein an orthographic projection of the first extension onto the base substrate has an area overlapped with an orthographic projection of the second extension onto the base substrate.

20. The electroluminescent display panel as claimed in claim **19**, wherein the orthographic projections of the first extension and the second extension onto the base substrate are partly overlapped with each other, and wherein the array substrate further comprises a metal electrode connected with the first extension or the second extension, wherein an orthographic projection of the metal electrode onto the base substrate is at most overlapped with the orthographic projection of one of the first extension and the second extension onto the based substrate.

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专利名称(译)	阵列基板，电致发光显示面板和显示装置		
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摘要(译)

公开了一种阵列基板，电致发光显示面板和显示装置。阵列基板包括：基础基板，第一信号线，绝缘层和第二信号线，在垂直于基础基板的方向上顺序设置在基础基板上;其中第一信号线具有第一部分和第二部分，第一部分的电阻高于第二部分的电阻，第一部分的至少一部分与第二信号线重叠，第二部分的第二部分的电阻高于第二部分的电阻与第二信号线不重叠。